Remarks/Arguments

Claims 1-20 are pending in the application. Claims 1-13 and 16-20 are allowed. Claims 14 and 15 stand rejected, and have been cancelled, without prejudice, from the application.

Applicant notes the Examiner's rejections of claims 14 and 15 and addresses these rejections below.

The Examiner has argued claims 14 and 15 are anticipated under 35 U.S.C. section 102(b) under Hayward (U.S. 4,720,324) or Mack (U.S. 4,104,111), and are anticipated under 35 U.S.C. section 102(e) by Pommer (U.S. 6,242,078 B1). The Examiner contends that these references teach an article and the article comprises the same structure regardless of the forming process. However, the Examiner bases his reasons on the same contentions which applicant addressed in its response to the previous Office Action.

Turning to the Examiner's rejection with respect to Hayward, Hayward discloses a process for the manufacture of a circuit board. The Examiner's description of what Hayward allegedly teaches does not appear to be consistent with the disclosure of Hayward. Contrary to the Examiner's statement in the Office Action (see page 2, paragraph 1, line 6-7), the covering mask (180) is not placed over the solderable areas, because the exposed areas (160) are built up to a solder area with a solderable surface (tin lead layer 190), made for terminal pads (col. 5, lines 5-6 of

Hayward). While the Examiner appears to state in the Office Action, on page 2, paragraph 1, line 7, that mention is made in Hayward of a functional layer used for edge connectors (e.g. made of gold)(col. 6, lines 44-46), there appears to be no teaching, suggestion or disclosure in Hayward of the process of creating such functional layers.

In addition, the Examiner appears to misinterpret Hayward when the Examiner states (page 2, paragraph 1, lines10-11 of the Office Action) that a solder mask would be applied and functional areas would be formed, referring to Hayward at col. 5, line 35 – col. 6, line 20. Again, the Examiner appears to equate the solder areas (160) to functional areas. However, the only functional areas which appear to be mentioned in Hayward may be the edge connectors (see col. 6, lines 44-46). Furthermore, contrary to the Examiner's statements at page 2, paragraph 1, line 12 through page 3, line 1 of the Office Action, Hayward does not disclose removal of the Sn-layer before formation of a function area. It appears that the use of the terms functional and solderable by the Examiner is not consistent with the use of these terms according to the present invention and applicant's disclosure. Therefore, applicant notes that the present process is different and distinguishable over Hayward and applicant reiterates that the characterization of Hayward by the Examiner in the current Office Action, for the same reasons as set forth by applicant in its response to the previous Office Action, and for the reasons set forth above, does not fairly

disclose, suggest or teach what the Examiner has characterized and purported that Hayward provides.

The Examiner has also relied on Mack in arguing a rejection in the current Office Action. (See, in particular, page 3, paragraph 2, lines 6-8 of the Office Action.) There, the Examiner states that a covering mask is placed over the solderable areas, leaving the functional areas exposed. But, in fact, the covered area is area (14) which is specified as a circuit trace (see col. 6, lines 35-36). Therefore, this area is not a solder region. However, connector areas are mentioned, which may be function areas. The method of forming connector areas is not taught, suggested or disclosed in the Mack specification or drawings. Contrary to the Examiner's statement, the exposed area (15) of Mack would refer to a solder region (terminal pad area--see col. 6, lines 36-37) rather than to a function region. Therefore, the solderable surface is not covered during the process of Mack which is opposite of the present invention, where the solderable surface is covered. The Examiner also makes an additional statement on page 3, paragraph 2, lines 8 and 9 of the Office Action, where the Examiner cites Mack (col. 7, lines 36-66) contending that Mack discloses the creation of a functional surface by chemical reduction. However, this does not appear to be disclosed by Mack, and, in particular, the citation referred to by the Examiner, since the respective citation refers to the creation of the solderable surface and not to the functional surface. As applicant previously pointed out in its

response to the prior Office Action, the present invention is distinguishable over Mack and is different than the process of Mack. Applicant for the reasons set forth in the previous response and above submits that Mack does not disclose or suggest the applicant's present invention.

The Examiner has cited U.S. Patent 6,242,078 B1(Pommer) as anticipating claims 14 and 15. Pommer actually relates to a method and apparatus for providing a high density printed circuit substrate. The substrate comprises a dielectric layer, which is to be provided with circuit traces. On page 4, paragraph 3, lines 9-10 of the Office Action, the Examiner states that a covering mask would be placed over the solder area leaving function areas exposed. Following the whole process, as explained in Applicant's prior Response, dated March 6, 2003, which was submitted in response to the previous Office Action, in Pommer there are no solder ***and*** function areas on the substrate present at the same time. In fact, the process disclosed by Pommer ends up with a circuit substrate, which is, in principle, the base material used for the process according to the present invention. Therefore, Pommer does not anticipate the present invention, nor does it suggest or disclose the applicant's invention which, if Pommer were employed at all, would be to provide a circuit substrate, which is only the starting material of the present invention. Accordingly, the Examiner's statement on page 4, paragraph 3, lines 3-4, 10-12, where the Examiner contends that Pommer would teach a process for producing a

solderable surface (pad) and a functional surface, and that further functional surfaces would be created by chemical reduction (electroless plating) of a metal, also fails to teach or disclose the applicant's invention, since the respective citation only refers to copper to be electroplated, and further after formation of solder areas and functional surfaces, the masking material (resist) would be removed.

In addition, the end product of Pommer is completely different than the end product of the process according to the applicant's present invention. The Examiner's position, on page 5, paragraph 6, lines 1-3, that Pommer allegedly teaches the article and the article comprises the same structure regardless of the forming process is not correct. Moreover, the starting materials in both cases are different, therefore, the present invention must be different from any invention disclosed in Pommer. Furthermore, in contrast to the present invention, there are no solder regions and function regions on the dielectric substrate at the same time in Pommer. Therefore, the end product of the present invention is not the same as that which is disclosed and relied upon by the Examiner in Pommer.

The Examiner's treatment of Pommer appears to be inconsistent with what Pommer actually and fairly discloses. The process and end product of Pommer are not sufficient to disclose or suggest the applicant's present invention.

Applicant submits the remarks herein to more particularly address the Examiner's statements.

Applicant having cancelled claims 14 and 15, the only claims which are not currently allowed, respectfully submits that all objections and rejections have now been overcome and that the case should be allowed. Early allowance of the pending claims is earnestly solicited.

If necessary, an appropriate extension of time to respond is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required to Patent Office Deposit Account No. 05-0208.

Respectfully submitted,
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